



UNIVERSITÀ DI PISA  
DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE  
Dottorato di Ricerca in Ingegneria dell'Informazione

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Doctoral Course

**“Design Technologies for Embedded Multiprocessor Systems-on-Chip”**

Prof. Dr. Rainer Leupers

*RWTH Aachen University - Germany*

**Short Abstract:** The trend towards Multicore and even Manycore architectures affects virtually all areas of computing today. Especially in the mobiles and consumer domains, an extremely high architectural efficiency (MIPS/Watt) is required. In order to manage the complexity of multi-billion transistor IC designs with dozens of heterogeneous processing engines, advanced Electronic System Level (ESL) tools are required. ESL can be roughly subdivided into four categories: architecture modeling and optimization, application SW mapping, simulation and verification, and efficient processing element design. After a general introduction to embedded MPSoC (Multiprocessor Systems-on-Chip) architectures and ESL technologies, the course will cover aspects from the above four domains, in particular SoC architecture exploration, embedded SW development with virtual platforms, efficient code generation for DSPs, and application-specific processing element design. The lectures will be complemented with hands-on lab sessions using modern industrial ESL tools. On the last day, a written final test will be offered.

**Course Contents in brief:**

- Multiprocessor Systems-on-Chip
- Electronic System Level Design
- SoC architecture exploration and power estimation
- Virtual Prototyping
- Multicore programming tools
- Application-specific processing elements (ASIPs)

**Total # of hours:** 20

**References:**

A. Hoffmann, H. Meyr, R. Leupers: Architecture Exploration for Embedded Processors with LISA, Kluwer Academic Publishers, ISBN 1-4020-7338-0, Dec 2002

P. lenne, R. Leupers (eds.): Customizable Embedded Processors: Design Technologies and Applications, Morgan Kaufmann, Series in Systems on Silicon, ISBN 0-1236-9526-0, Jul 2006

R. Leupers, O. Temam (eds.): Processor and System-on-Chip Simulation, Springer, ISBN 978-1-4419-6174-7, Sep 2010

J. Castrillon, R. Leupers: Programming Heterogeneous MPSoCs: Tool Flows to Close the Software Productivity Gap, Springer, ISBN 978-3319006741, July 2013

S. Schuermans, D. Zhang, D. Auras, R. Leupers, G. Ascheid, X. Chen, L. Wang: Creation of ESL Power Models for Communication Architectures using Automatic Calibration, 50th Design Automation Conference (DAC), Austin (USA), June 2013

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## **CV of the Teacher**

Rainer Leupers received the M.Sc. (Dipl.-Inform.) and Ph.D. (Dr. rer. nat.) degrees in Computer Science with honors from the Technical University of Dortmund, Germany, in 1992 and 1997. From 1997-2001 he was the chief engineer at the Embedded Systems chair at TU Dortmund. In 2002, Dr. Leupers joined RWTH Aachen University as a professor for Software for Systems on Silicon. Since then, he has also been a visiting faculty member at the ALARI Institute in Lugano. His research and teaching activities comprise software development tools, processor architectures, and system-level electronic design automation, with focus on application-specific multicore systems. He published numerous books and technical papers, and he served in committees of leading international conferences, including DAC, DATE, and ICCAD. He was a co-chair of the MPSoC Forum and SCOPES. Dr. Leupers received several scientific awards, including Best Paper Awards at DATE 2000, 2008 and DAC 2002, and he holds several patents on processor design automation technologies. He has been a co-founder of LISATek (now with Synopsys) and Silexica. He has served as consultant for various companies, as an expert for the European Commission, and in the management boards of compound research projects like UMIC, TETRACOM, HiPEAC, and ARTIST.

## **Room and Schedule**

Room: *Aula Riunioni del Dipartimento di Ingegneria dell'Informazione, Via G. Caruso 16, Pisa – Ground Floor*

### **Schedule:**

Day1 (14.07.2015): 9.30-17.30

Day2 (15.07.2015): 9.30-17.30

Day3 (16.07.2015): 9.30-17.30

Day4 (17.07.2014): 9.30-11.00 – Final Test