UNIVERSITÀ DI PISA

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

Dottorato di Ricerca in Ingegneria dell'Informazione

Doctoral Course

"Reconfigurable Hardware, Tools and Applications"

Prof. Michael Huebner

Brandenburg University of Technology, Germany

Short Abstract: Reconfigurable hardware enables to develop digital circuits and configure a FPGA device. The hardware itself is "reconfigurable" which means, that the circuit can be adapted, if for example a change is needed caused by a modification of the specification of a system. Modern architectures allow to modify the configuration of the chip even during run-time. This so called dynamic and partial reconfiguration opens several opportunities for run-time adaptive system. The course introduces reconfigurable hardware architectures and shows how to develop systems which have the capability to be run-time adaptive. Several applications will show the benefit of this methodology.

Course Contents in brief:

- Traditional processor architectures
- Hardware / Software Codesign
- Adaptive processor systems
- Run-time adaptation of systems

Total # of hours of lecture: 12h

References:

[1] **Computer Architecture, 6th Edition, A Quantitative Approach, John Hennessy and David Patterson**

[2] Reconfigurable Computing: From FPGAs to Hardware/Software Codesign, J. Cardoso and M. Hübner

CV of the Teacher

Prof. Dr.-Ing. habil. Michael Hübner is full professor at the Brandenburg University of Technology - Cottbus - Senftenberg. He is leading the Computer Engineering Group since October 2018. From 2012-2018 he lead the Chair for Embedded Systems for Information Technology (ESIT) at the Ruhr-University of Bochum (RUB). He received his diploma degree in electrical engineering and information technology in 2003 and his PhD degree in 2007 from the University of Karlsruhe (TH). Prof. Hübner did his habilitation in 2011 at the Karlsruhe Institute of Technology (KIT) in the domain of reconfigurable computing systems. His research interests are in reliable and dependable reconfigurable computing and particularly new technologies for adaptive FPGA run-time reconfiguration and on-chip network structures with application in automotive systems, incl. the integration into high-level design and programming environments. Prof. Hübner is main and co-author of over 250 international publication. He is in the steering committee of the IEEE Computer Society Annual Symposium on VLSI, organized more than 25 events like workshops and symposia, and is active as guest editor in many journals like e.g. IEEE TECS, IEEE VCAL and IEEE TNANO.

Room and Schedule

Room: *Aula Riunioni del Dipartimento di Ingegneria dell'Informazione, Via G. Caruso 16, Pisa – Ground Floor*

Schedule:

Monday 13 May – 14.00 -18:00

Tuesday 14 May – 09:00 – 13:00

Wednesday 15 May – 09:00 – 13:00