UNIVERSITÀ DI PISA

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

Dottorato di Ricerca in Ingegneria dell'Informazione

Doctoral Course

"Ultra-low power integrated systems for green growth to the trillion scale"

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Short Abstract

The course focuses on ultra-low power integrated circuit design for distributed and decentralized systems (e.g., IoT, AIoT), and in particular on the design of chips for edge nodes. The course provides an insight into system requirements imposed by real-world applications, the fundamentals to understand the related challenges, and advanced design ideas to address them. Several aspects are discussed from a design viewpoint, ranging from ultra-low power system architectures, architectures and circuits for processing, data sensemaking (e.g., machine learning on a chip), energy harvesting, on-chip power conversion, sensor interfaces and wireless communications.

The course is structured into three sections. In the first one, fundamentals on ultra-low power and minimum-energy design are provided as common background. Key concepts, models and techniques are presented to enable intelligent systems with divergently high peak performance and low minimum power, as relevant to current and prospective applications of distributed/decentralized systems. In the second section, recent techniques that drastically extend the performance-power scalability of intelligent systems are presented. Silicon demonstrations of better-than-voltage-scaling adaptation to the workload are illustrated for the entire signal chain from sensors to sensemaking. Demonstrations include the data and the clock path of the digital sub-system, the analog sub-system and power management. Energy-quality scaling is explored as additional dimension to break the conventional performance-energy tradeoff in error-resilient applications such as AI and vision, from networks on chip to memories and accelerators. Further performance and energy improvements are discussed through uncommonly flexible in-memory broad-purpose computing frameworks for true data locality, from buffering to signal conditioning and neural net workloads. In the third section, adaptation to an even wider range of power-performance targets is presented to shrink and eventually suppress batteries as fundamental obstacle to overcome in the exponential scaling towards trillions of devices (environmental, economics, logistics). Sensor interfaces, processors and wireless transceivers fitting existing infrastructure (e.g., WiFi) with power reductions by orders of magnitude are discussed and exemplified by numerous silicon demonstrations, and their system integration.

In this course, all design principles are exemplified by silicon demonstrations from the state of the art, and with extensive measurement results from our research group to closely mimic the learning experience in a lab environment. As further learning tool, databases of commercial products and

state-of-the-art research prototypes are introduced and offered to the attendees to understand the trends, the requirements and the advances taking place in the field. The lecture notes are complemented by springer books available in most university libraries in electronic form to extend the learning journey beyond the course. The attendees should have some basic understanding of electronic circuits and integrated circuits and/or systems.

Course Contents in Brief

- SECTION I: Fundamentals of ultra-low power design for intelligent self-powered systems
- SECTION II: Design frameworks and techniques for aggressive power-performance tradeoff extension
- SECTION III: Green and alert integrated systems without battery for environmental, technological, economic and logistic sustainability towards the trillion scale

Total # of hours of lecture: 16

References:

[1] M. Alioto (Ed.), Enabling the Internet of Things – from Integrated Circuits to Integrated Systems, Springer, 2017

[2] S. Jain, L. Lin, M. Alioto, Adaptive Digital Circuits for Power-Performance Range beyond Wide Voltage Scaling, Springer, 2020

CV of the Teacher

Massimo Alioto (M'01–SM'07-F'16) received the Laurea (MSc) degree in Electronics Engineering and the Ph.D. degree in Electrical Engineering from the University of Catania (Italy) in 1997 and 2001, respectively. He is a Professor at the Department of Electrical and Computer Engineering, National University of Singapore where he leads the Green IC group and is the Director of the Integrated Circuits and Embedded Systems area as well as the FD-FAbrICS research center. Previously, he held positions at the University of Siena, Intel Labs – CRL (2013), University of Michigan Ann Arbor (2011-2012), BWRC – University of California, Berkeley (2009-2011), and EPFL (Switzerland, 2007).

He has authored or co-authored more than 330 publications on journals and conference proceedings. He is co-author of five books, *In-Memory and Immersed-in-Logic Primitives for Ubiquitous Hardware Security* (Springer, 2022), *Adaptive Digital Circuits for Power-Performance Range beyond Wide Voltage Scaling* (Springer, 2020), *Enabling the Internet of Things - from Circuits to Systems* (Springer, 2017), *Flip-Flop Design in Nanometer CMOS - from High Speed to Low Energy* (Springer, 2015) and *Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL and SCL Digital Circuits* (Springer, 2005). His primary research interests include self-powered wireless integrated systems, green computing, widely energy-scalable integrated systems, data-driven integrated systems, hardware-level security, and emerging technologies, among the others.

He is the Editor in Chief of the IEEE Transactions on VLSI Systems (2019-2022), and was the Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. He is/was Distinguished Lecturer of the IEEE Circuits and Systems Society (2022-2023, 2009-2010) and Solid-State Circuits Society (2020-2021). He was also member of the Board of Governors of the IEEE

Circuits and Systems Society (2015-2020), and Chair of the "VLSI Systems and Applications" Technical Committee (2010-2012). In the last five years, he has given 50+ invited talks in top conferences, universities and leading semiconductor companies. He served as Guest Editor of several IEEE journal special issues (e.g., TCAS-I, TCAS-II, JETCAS). He also serves or has served as Associate Editor of a number of IEEE and ACM journals. He is/was Technical Program Chair (ISCAS 2023, SOCC, ICECS, NEWCAS, VARI, ICM, PRIME) and Track Chair in a number of conferences (ICCD, ISCAS, ICECS, VLSI-SoC, APCCAS, ICM). Currently, he is also in the IEEE "Digital architectures and systems" ISSCC subcommittee, and the IEEE ASSCC technical program committee. Prof. Alioto is an IEEE Fellow.

Room and Schedule

Room: *Aula Riunioni del Dipartimento di Ingegneria dell'Informazione, Via G. Caruso 16, Pisa – Ground Floor*

Schedule:

- Day1 20/06/2022 – 9:00-15:30 (6 hours): megatrends and perspectives on distributed/decentralized systems, requirements, recap of circuit models, design for nearly-minimum energy operation.
- Day2 21/06/2022 – 9:00-15:30 (6 hours): background on power-performance tradeoff in intelligent and always-on systems, techniques to extend of power-performance range beyond voltage scaling from data path to clock path, energy-quality scaling and application to main sub-systems, in-memory computing, case studies.
- Day3 22/06/2022 – 9:00-14:00 (4 hours): trends and need for battery suppression (environment, economics), integrated energy sources, system powering/activation schemes, battery-indifferent and battery-less system architectures, circuit techniques for main sub-systems, case studies.