UNIVERSITÀ DI PISA

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

Dottorato di Ricerca in Ingegneria dell'Informazione

Doctoral Course

"Arm Architectures for High-Performance Real-Time"

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Short Abstract:

The evolution of computer systems is bringing them constantly closer to the physical world by making machines interact with their surrounding reality. Industrial automation, robotics, aerospace and automotive industries drive increasing demands on both deterministic capabilities and compute performance into the Arm computer systems architecture.

This course will introduce elements of the Arm systems architecture and current and future solutions Arm is adopting, together with its partners, to enable the next generation of high-performance real-time computing.

The audience will be introduced to the Arm real-time compute activities, and how those activities will significantly impact all market segments where both performance and determinism are requirements.

Course Contents in brief:

- Introduction to Arm and the Arm Architecture
- System Architecture and Composition
- Heterogeneous multi-core platforms
- The shared resources interference problem in high performance real-time systems
  - Shared caches
  - Shared interconnect
  - Shared memory
  - Other: SMMU, accelerators, interrupt controller
- Introduction to modelling Heterogeneous platforms on gem5
- Introduction to Adaptive Traffic Profiles

Total # of hours of lecture: 16

References:

Introducing the Arm architecture v.10, ARM062-948681440-3277, https://developer.arm.com/architectures/learn-the-architecture/introducing-the-arm-architecture/single-page

The gem5 simulator, ACM SIGARCH Computer Architecture News, August 2011 https://doi.org/10.1145/2024716.2024718

AMBA Adaptive Traffic Profiles Specs: https://www.arm.com/resources/guide/amba-adaptive-traffic-profiles

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CV of the Teacher

Matteo Andreozzi got his PhD in Information Engineering at the University of Pisa, Italy, in 2012, advised by prof. Lenzini and prof. Stea, defending a thesis on QoS algorithms for 3.5G and 4G cellular networks.
He has been with Arm, Cambridge (UK) since 2015, and he now leads Arm's Future System Design (FSD) Real Time Architecture team. The team is tasked with designing solutions for mobile, automotive, embedded, industrial and robotic systems, considering QoS, real-time guarantees and performance of Arm based systems.
From 2012 to 2015 he was with Nvidia, in the Algorithm and Standards group, developing code for an LTE network simulator, and evaluating and improving the performances of Nvidia's current and future products.
He co-authored more than 10 scientific papers and six international patents. He has recently co-authored an invited paper at COMPSAC 2020, and he is scheduled to hold a keynote at ECRTS 2020 in Modena. He organized the first Arm High-performance Real-time Workshop in Cambridge in 2019.

Room and Schedule

Room: *Aula Riunioni del Dipartimento di Ingegneria dell'Informazione, Via G. Caruso 16, Pisa – Ground Floor*

Schedule:

Day 1 (half day)

- Introduction to Arm and the Arm Architecture
  - History of Arm, current business models, markets, organization
  - The concept of Arm Partnership and Ecosystem
  - The Arm architecture: what is it, what is it for
- System Architecture and Composition
  - Designing an Arm-based system, the role of the system architect
- Heterogeneous multi-core platforms
  - Challenges and opportunities of next-generation compute platforms

Day 2 (full day)

- The shared resources interference problem in high performance real-time systems
  - Shared caches
    - Introduction to caches
    - Points of contention, observability, controllability
  - Shared interconnect
    - Introduction to interconnects
    - Points of contention, observability, controllability
  - Shared memory

        - Introduction to main memory
        - Points of contention, observability, controllability
    - Other: SMMU, accelerators, interrupt controller
        - Overview of other shared resources, their characteristics and problematics

Day 3 (half day)

- Introduction to modelling Heterogeneous platform on gem5 and Adaptive Traffic Profiles
    - The gem5 simulator
- Introduction to Adaptive Traffic Profiles
    - ATP as a way to capture the dynamic behavior of memory devices